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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,642	08/13/2001	Andrew J. Walker	035905-0103	8019

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,642	WALKER ET AL.	
	Examiner	Art Unit	
	Evan Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) *13-18,21-24 and 27-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-12,19,69 and 70* is/are rejected.

7)☒ Claim(s) *20,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed February 20, 2004, with respect to the rejection of claims 1-12, 19, 20 and 69 under 35 USC 103(a) have been fully considered and are persuasive (in view of new evidence introduced by applicant after Final Rejection).

Accordingly, the rejection under 35 USC 103(a) has been withdrawn.

However, upon further consideration, a new ground of rejection is made in view of the newly discovered reference to Iida et al. (U.S. 5,747,846).

2. In view of the Appeal Brief filed on February 20, 2004, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (since this Office action is non-final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 7, 8, 19, 69 and 70 are rejected under 35 U.S.C. 102(b) as being anticipated by Iida et al. (US 5,747,846).

Regarding claim 1, Iida et al. discloses a nonvolatile memory array (e.g. col. 9, lines 19-24), comprising: an array of nonvolatile memory devices (e.g. EPROM); at least one driver circuit (e.g. col. 6, lines 11-15); and a substrate (e.g. 1); wherein the at least one driver circuit is not located in a bulk monocrystalline substrate (because it is located in an SOI substrate per col. 6, line 13).

Regarding claim 2, Iida et al. point out that "it is preferable to fabricate the [driver] circuit by an SOI process" [col. 6, lines 11-15]. Therefore, the driver circuit is necessarily "in a SOI substrate."

Regarding claim 5, Iida et al. disclose wafer bonding as one possible choice [e.g. col. 6, line 63].

Regarding claim 7, the driver is located over monocrystalline substrate 1 (i.e. the substrate which was used to form the SOI substrate having insulator layer 2).

Regarding claim 8, the driver circuit is separated from the substrate 1 by an insulating layer 2.

Regarding claim 19, EEPROM arrays are "one preferred embodiment" (col. 3, lines 59-61).

Regarding claim 69, Iida et al. disclose a nonvolatile memory array (e.g. col. 9, lines 19-24), comprising: an array of nonvolatile memory devices (col. 1, lines 17-20); a silicon on insulator substrate (col. 6, lines 51-65); and at least one memory driver circuit located in the silicon on insulator substrate (e.g. col. 6, lines 6-15).

Regarding claim 70, Iida et al. disclose that the nonvolatile memory devices are transistors each comprising a charge storage medium (e.g. "floating gate transistor" per col. 4, lines 46-51 store charge in the floating gate medium).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4, 6 and 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al. as applied to claim 1 above, and further in view of applicant's admitted prior art of record.

Iida et al is silent about "SIMOX," "seeded lateral epitaxy," a polycrystalline silicon on insulator SOI, or that the driver is formed above a "glass," "plastic," or "ceramic" substrate.

However, applicant admits that "SIMOX," "seeded lateral epitaxy," polycrystalline silicon on insulator, and use of plastic, glass and sapphire for SOI substrates were "all known" for making an SOI substrate. Furthermore, applicant does not distinguish anything unexpected among the types of prior art SOI technology contemplated: Quoting applicant:

> Various techniques are known for forming an SOI substrate. All result in a silicon on an insulator. Depending on the method of formation, the silicon layer can be crystal, polycrystalline, or amorphous. The substrate can be monocrystalline silicon (with an intervening insulator) or some insulating material, such as glass plastic or ceramic. [Brief on Appeal filed February 20, 2004, p. 3, 5th paragraph, emphasis added].

Thus, applicant admits that the limitations of claims 3-4, 6 and 9-12 "all result in a silicon on insulator."

We know that Iida et al. specifically disclose the advantage of a driver circuit in a silicon on insulator (SOI) substrate being better "insulating isolation and breakdown voltage" (col. 6, lines 11-15), and also makes the statement that "it is preferable to fabricate the [driver] circuit by an SOI process" [col. 6].

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt any "known" process for forming an SOI substrate, wherein one would be motivated to reap the benefits of a driver circuit in SOI, being better insulating isolation and breakdown voltage [col. 6, lines 6-15].

Art Recognized Equivalence for the Same Purpose

Applicant's limitations drawn to known methods and materials for "SOI" to not render the claims patentably distinct from Iida et al.. Applicant states that "all result in SOI" with respect to claim limitations drawn to material choice and process steps for making a SOI substrate. Since the cited prior art discloses that "SOI is preferable" for a "driver circuit," SOI by any method or material choice can properly be considered an art recognized equivalent, particularly since applicant does not demonstrate anything novel or unexpected by the "known" choices claimed for the "SOI" preferred by Iida et al.. Iida directs one of ordinary skill to "SOI" but is silent about all the known equivalents for SOI [See MPEP 2144.06].

Allowable Subject Matter

5. Claims 25-26 are objected to for depending on a rejected claim, but are otherwise allowable for reasons of record in the last Office Action.

6. Claim 20 is also objected to for depending on a rejected claim, but is now found to be otherwise allowable because claim 20 distinguishes from prior art particularly by the additional limitation that the claimed nonvolatile memory devices (having a driver circuit not located in a bulk monocrystalline substrate) comprise a monolithic three dimensional array of memory devices (wherein Iida et al. only disclose written description for a 2-dimensional array of memory devices).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
May 15, 2004

EVAN PERT
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